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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,315	10/25/2001	Seong Yong Kim	8111-009-999	2983

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EXAMINER	
ELMORE, REBA I	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 07/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,315	KIM, SEONG YONG	
	Examiner	Art Unit	
	Reba I. Elmore	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6,7 and 10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,7 and 10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4, 6-7 and 10 are presented for examination.

2. The finality of the previous office action is vacated. The amendment filed June 8, 2005 has been entered.

SPECIFICATION

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

5. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

35 USC § 112, 2nd paragraph

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-4, 6-7 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 1 uses an upper address bit, however, further in the body of the claim 'the upper address' is referred to and not specifically the upper address bit of the register block. This indistinct limitation applies to all claims dependent upon independent claim 1.

9. Claim 7 states 'signals inputted to the memory card module of the hierarchical memory configuration are compensated again at memory module and memory block stages' which does not constitute a definite limitation being particularly pointed out or distinctly claimed. The signals being input are unclear in nature and the repetition of some type of compensation to either the memory card module or the signals themselves is equally unclear and indistinct.

10. The previously given rejections of claims 1-10 and 12-13 as being indefinite are ***withdrawn***.

35 USC § 102

11. The rejection of claims 1-8 as being anticipated by Gates is ***withdrawn***.

35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1-4, 6-7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horan et al.

14. Horan teaches the invention (claim 1) as claimed including a system for addressing a data storage unit used in at least a server or client computer, the system comprising:

means for converting a format of data on an external bus such that the data are accessed on an internal bus for use in the system as the core logic which allows data from different memories to be used by the system (e.g., see Figure 2, element 204 and col. 10, lines 37-67);

a memory card module connected to the internal bus for storing data transmitted through the internal bus, wherein the memory card modules includes a plurality of memory modules each having a plurality of equally-sized memory blocks, each memory block being divided into a predetermined number of equally-sized sub-memories such that the memory module has a hierarchical memory configuration, wherein the memory card module includes a PCI-to-memory controller, which is disposed between the internal bus and the memory module as a bridge, for controlling access to the plurality of sub-memories as the typical functionality of the PCI/IDE controller, PCI/EISA/ISA bridge, PCI/SCSI bus adapter type of devices (e.g., see Figure 2, 2A, elements 118, 116 and 114 and col. 10, lines 37-54) with there being several indications of using 4 kilobyte page sizes (e.g., see col. 10, lines 2-8, col. 16, lines 1-56 as well as other parts of the reference);

wherein the PCI-to-memory controller includes:

a PCI interface controlling unit for performing a standard PCI command, control and data signal processing as the typical functionality of the PCI/IDE controller, PCI/EISA/ISA bridge, PCI/SCSI bus adapter type of devices (e.g., see Figure 2, 2A, elements 118, 116 and 114 and col. 10, lines 37-54), the PCI interface controlling unit including a register block with a base address register being equivalent to the register block of the claim, the base address register is used in the system BIOS memory mapping for allocating address space (e.g., see col. 12, line 65 to col. 15, line 5) the select bit is used to directly access the memory module is inherent as the figures and description (e.g., see col. 2, lines 38-49) show using integrated circuit technology which indicates using memory chips thereby requiring select bits for selecting, choosing and/or activating the use of the memory chip; and

a plurality of memory controlling units for performing a direct read/write operation for the sub-memories in response to the PCI command from the PCI interface controlling unit as using PCI/SCSI bus adapters, PCI/EISA/ISA bridges, PCI/IDE controllers and PCI/PCI bridges for transferring data using various types of buses in order to read and write data to and from CD ROMs, NVRAMs, tape memory and disk memory as well as ports which represent connectivity to other types of memory devices as well as network connectivity (e.g., see Figures 2, 2A and 3 and col. 10, line 37 to col. 12, line 18); and,

means for writing data on the internal bus to the memory module and reading out the data therefrom as using the primary PCI bus, element 109, connected to the core logic to the memory bus, element 105, which is connected to the system RAM and which allow writing data and reading data to/from the various memory devices shown (e.g., see Figure 2, 2A and col. 10, lines 37-67).

The Horan reference does not specifically teach using a lower address bit, an upper address bit and a select bit wherein the lower address bit represents addresses included in the range of an address region within a memory map, the upper address bit represents an address set to be used when a memory address region is beyond the address region of the memory map, however, the reference teaches using address maps detailing how address space is to be used by the system. Base address registers are taught which use the value from the least significant bit to the most significant bit for indicating an address range for the use in mapping the use of the memory. The mapping is specifically taught in relationship to a graphics controller but is applied to other devices in the system. The various figures give details of the memory mapping, memory translations and remapping. It would have been obvious to one of ordinary skill in the

art at the time the invention was made to use specific address bits to indicate the address mapping to be used by the various controllers and devices in the system.

As to claim 2, Horan teaches the internal bus is a PCI interface bus (e.g., see Figure 2).

As to claim 3, Horan teaches the external bus is a SCSI bus (e.g., see Figure 2, element 111) with a PCI/SCSI bus adapter also being shown (e.g., see Figure 2, element 114).

As to claim 4, Horan teaches the memory card module is composed of any one of SDRAM, Rambus DRAM, DDR or other equivalent memories (e.g., see col. 11, lines 41-57).

As to claim 6, Horan teaches the predetermined number is four as the reference teaching using 4KB sizes for memory pages.

As to claim 7, Horan teaches signals inputted to the memory card module of the hierarchical memory configuration are compensated again at memory module and memory block stages as being inherently taught as the memory card modules receive the necessary signals to use the memory card modules in the system.

As to claim 10, Horan teaches the PCI-to-memory controller activates any of the plurality of sub-memories to be actually accessed and maintains the remaining in a low power mode as being inherent and well known and official notice is taken thereof. Horan specifically states in the description of the related technology using the invention in a wide variety of different computers including portable lap-top computers. Lap-top computers are well known to have a sleep or inactive mode which is a low-power mode for maintaining data in memory modules which require refreshing for the data to be kept coherent.

CONCLUSION

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (571) 272-4192. The examiner can normally be reached on M-TH from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2187, Donald Sparks, can be reached for general questions concerning this application at (571) 272-4201. Additionally, the official fax phone number for the art unit is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center central telephone number is (571) 272-2100.

Reba I. Elmore
Primary Patent Examiner
Art Unit 2187

July 6, 2005